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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
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| 09/998,241 | 12/03/2001 | Philip Joseph Koh | A8250 | 6210 |

7590 11/26/2002

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| EXAMINER |
|---|
| MAGEE, THOMAS J |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2811 | |

DATE MAILED: 11/26/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 09/974,962 | TAKAHASHI ET AL. | |
| | Examiner | Art Unit | |
| | VanThu Nguyen | 2824 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☐ Responsive to communication(s) filed on _____ .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *4-9 and 14-18* is/are allowed.

6)☒ Claim(s) *1-3,10-13 and 19* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *12 October 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

**Priority under 35 U.S.C. §§ 119 and 120**

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☒ Certified copies of the priority documents have been received in Application No. *08/574,104* .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☒ Other: *Search Report* .

## DETAILED ACTION

1. This present applicant is reissue applicant of serial number 08/982,398.

2. Claims 1-19 are pending.

3. Claims 10-19 are newly added.

### *Claim Objections*

4. Claims 2-3, 5-6, 8-9, 11-12, 14-15, 17-18 are objected to because of the following informalities: "A semiconductor memory" in line 1 of each claim. Appropriate correction is required, such as --The semiconductor memory--.

### *Claim Rejections - 35 USC § 112*

5. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

6. Claim 10-12 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 10 recites the limitation "said third regions" in line 18. There is insufficient antecedent basis for this limitation in the claim.

Claim 10, lines 13-16, is different from claim 1 of original application.

### *Claim Rejections - 35 USC § 102*

7. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in-
> (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in

section 351(a) shall have the effect under this subsection of a national application published under section 122(b) only if the international application designating the United States was published under Article 21(2)(a) of such treaty in the English language; or
(2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that a patent shall not be deemed filed in the United States for the purposes of this subsection based on the filing of an international application filed under the treaty defined in section 351(a).

8. Claims 1-3, 10-12, 19 are rejected under 35 U.S.C. 102(e) as being anticipated by Ikeda et al. (U.S. Patent No. 6,307,217).

Regarding claim 1, Ikeda et al. disclose a semiconductor memory comprising:

a plurality of first regions arranged in lattice fashion (SMA, see FIG. 2), each of which corresponds to a memory array including a plurality of main word lines (MWL, see FIG. 2) extending in a first direction (horizontal), a plurality of sets of sub-word lines (SWL, see FIG. 3) extending in said first direction, a plurality of pairs of data lines (complementary data lines DLs, see FIG. 3) extending in a second direction (vertical) perpendicular to said first direction and a plurality of memory cells, each of which is coupled to a corresponding one of said plurality of sub-word lines and a corresponding one of said data lines, one of said plurality of main word lines being allotted to one of said plurality of sets of sub-word lines (see column 11 lines 1-23);

a plurality of second regions (WDEC, see FIG. 3), each of which is arranged alternately with each of said first regions arranged along said first direction and each of which includes sub-word line drivers connected to said sub-word lines (a WDEC is located at one end of each of SMA, see column 11, lines 1-2).

a plurality of third regions (YSW, YDEC, SA, see FIG. 3), each of which is arranged alternately with each of said first regions arranged along said second direction and each of which includes sense amplifiers (SA, see FIG. 3) connected to said data lines; and

a plurality of fourth regions (regions between where DATA BUS running across, see FIG. 3), each of which is arranged alternately with each of said third regions arranged along said first direction, wherein each of said plurality of main word lines extends through one or more of said first regions arranged along said first direction;

wherein said semiconductor memory further includes:

a plurality of pairs of sub-common data lines (vertical output lines from SA, see FIG. 3), each of which extends through said third regions arranged along said first direction (plurality of sub-common data lines being arranged one by one in horizontal direction).

first switching circuits (YSW, see FIG. 3) formed in said third regions and connected interposingly between said plurality of pairs of data lines and a corresponding one of said pairs of sub-common data lines;

a plurality of pairs of main-common data lines (DATA BUS, see FIG. 3), each of which extends through one or more of second regions arranged along said second direction (plurality of DATA BUS being arranged one by one in vertical direction); and

second switching circuits (MP, see FIG. 27) formed in said fourth regions and connected interposingly between a corresponding one of said pairs of main-common data lines and a corresponding one of said pairs of sub-common data lines.

Regarding claims 2-3, Ikeda et al. further disclose a number of memory arrays allotted to one of said main word-lines (which is 32 SMA, see FIG. 2) is greater than a number of memory arrays allotted to a corresponding one of said pairs of sub-common data lines (which is ½ of

SMA, see FIG. 3); length of said each main word-line is longer than a length of said each pair of sub-common data lines (observing from FIGS. 2 and 3).

Regarding claims 10-12, they are rejected under U.S.C. 102(e) since they recite similar limitation as in claims 1-3, except replacing plurality pairs of data lines/sub-common data lines/main data lines with plurality of data lines/sub-common data lines/main data lines. However, "plurality of pairs of data lines/sub-common data lines/main data lines" can also be considered as "plurality of data lines/sub-common data lines/main data lines".

Regarding claim 19, Ikeda et al. disclose a semiconductor comprising a plurality of word lines layered by main word lines (MWL) and sub-word lines (SWL) (see FIG. 14); a plurality of I/O lines inherently layered by data lines (DLs), sub-common data lines (output from SA) connected to said data lines and main-common data lines (DATA BUS) connected to said sub-common data lines (see FIG. 3).

***Allowable Subject Matter***

9. Claims 4-9, 13/~~14~~-18 are allowed.

***Conclusion***

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to VanThu Nguyen whose telephone number is (703) 306-9121. The examiner can normally be reached on Monday-Thursday, 7:00am-4:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Richard Elms can be reached on (703) 308-2816. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 872-9318 for regular communications and (703) 872-9319 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

VTN
November 22, 2002

Van Thu Nguyen

VAN THU NGUYEN
PATENT EXAMINER